26.9 A 1.7GHz 1.5W CMOS RF Doherty Power Amplifier for Wireless Communications

Naratip Wongkomet, Luns Tee, Paul R. Gray

University of California, Berkeley, CA

Full integration of the PA at high efficiency has long been one of the most difficult challenges in achieving low-cost RF transceiver functions in CMOS. Supply voltage diminution as a result of CMOS technology scaling has made this even more difficult. Much of the recent work in CMOS PAs has been targeted at efficiency-enhancement techniques to compensate for the inherent limitations of CMOS technology [2]. A property shared among most PAs is that maximum power efficiency is achieved only when the PA is transmitting its peak output power. Efficiency worsens as output power decreases. Under typical operating conditions, the PA transmits much lower than its peak output power, therefore, the effective power efficiency is much lower than the maximum value. In this paper, a concept first developed in the vacuum-tube era by Doherty [1] to improve amplifier efficiency over a wide range of output power is applied to the CMOS PA problem. A prototype is described, embodying a fully differential 1.7GHz 1.5W Doherty PA in 0.13μm CMOS technology. A 3.3V supply is used in the output stages. The rest of the chip uses 1.2V supply. All components are integrated on a single CMOS die except for a capacitor in the output matching network. Bondwires are used in the output stages and the matching network to achieve high quality-factor (Q) inductances. They do not need precise trimming since the loaded Q of the output nodes is low.

The Doherty configuration consists of two sub-amplifiers, a main and an auxiliary amplifier, as shown in Fig. 26.9.1. During low output power operation, only the main amplifier is turned on. The main amplifier operates alone until its output power is limited by its maximum voltage swing, achieving the first efficiency peak. To realize increased output power beyond that, the auxiliary amplifier is also turned on. The key aspect of the Doherty configuration is the use of a passive impedance inverter network, Z_{inv}, to combine the output power from both amplifiers in a way that achieves low losses and does not require increased voltage swings.

With the phases of the two signal paths matched, the auxiliary amplifier increases the resistance seen by the Z_{inv} network upon its turning on. Due to impedance inversion, the load resistance seen by the main amplifier decreases, allowing the main amplifier to output more current and hence power while maintaining its maximum voltage swing. The second efficiency peak is achieved when the auxiliary amplifier output swing is also at the maximum. The overall efficiency remains high all the time that the auxiliary amplifier is turned on since the main amplifier operates at its maximum swing.

Both main and auxiliary amplifiers consist of three stages as shown in Fig. 26.9.2. They are designed to have an input capacitance of the 0.4pF and give approximately 40dB of power gain. Predrivers and drivers are implemented as common-source amplifiers with cascode transistors. Both predrivers also have tail current-source transistors to enhance common-mode rejection. The output stage of the main amplifier is designed as a class-AB amplifier whereas the output stage of the auxiliary amplifier is biased in a class-C region. Thick-oxide transistors are used in the output stages as cascode transistors for higher output swings. To prevent oxide breakdown, gates of the cascode transistors are biased close to V_{DD}. However, it allows the cascode transistor to enter triode region before the transconductance transistor, causing gain expansion across the Miller capacitance C_{gd} of the transconductance transistor. As a result, the input capacitance increases and can create significant distortion in the driving stage. Cross-coupled capacitors between gate and drain are added to neutralize this effect.

The Z_{inv} network is fully integrated and implemented as a lumped network instead of the conventionally used bulky quarter-wavelength transmission line [1]. A diagram of the Z_{inv} network is shown in Fig. 26.9.3. Output capacitance of both amplifiers can be absorbed into the network. For this prototype, the breakpoint where the auxiliary amplifier is turned on is designed to be at 9dB backoff from the peak output power. This is done by choosing L_{inv} such that its impedance is three times the load resistance R_L. Switched capacitor arrays are used to tune the impedance of C_{inv} to match that of L_{inv}. These arrays can also tune out the variation of bondwires at the output of both amplifiers. Power loss in the low-Q spiral inductor of this network directly degrades the overall efficiency. However, once the auxiliary amplifier is turned on, the current from the auxiliary amplifier through the spiral inductor counters that from the main amplifier, causing the ratio of the inductor loss to the output power to decrease. With the estimated spiral inductor Q of 8, insertion loss is 1.7dB during low output power operation and decreases to 0.25dB at peak power. This causes the first efficiency peak to be much lower than the second peak.

Since the Z_{inv} network inherently gives 90° phase shift, a polyphase circuit, consisting of matched resistors and matched capacitors, is used at the input to correct for this. A diagram of the polyphase circuit is shown in Fig. 26.9.4. The 90° phase difference at the output of the polyphase circuit is maintained at all frequencies regardless of resistor values, capacitor values, or load capacitance. However, the relative gain between the two paths is subject to variation due to process tolerances. This can be compensated by using NMOS resistors in parallel with the fixed resistors, achieving over 6dB of gain-adjustment range. In order to avoid distortion in these NMOS resistors, the input amplitude to this network is designed to be 0.15V.

This prototype is fabricated in a 0.13μm CMOS process with MIM capacitors. The die size is $2.8\times3.2mm^2$ including all on-chip bypass capacitors and pads. A micrograph is shown in Fig. 26.9.7. The maximum output power measured at 1.7GHz is 1.5W with a peak drain efficiency of 39%. The operating frequency is lower than expected due to larger than expected bondwire inductance. With the power consumption in the driving stages included, the peak PAE is 36% (33% combined with off-chip balun). The PAE stays above 18% over a 10dB range of output power. Figure 26.9.5 shows a plot of PAE versus output power. When tested with a GMSK modulated signal, the output spectrum fits under the GSM spectral mask at all output power levels with a maximum peak phase error of 1.2°.

Acknowledgements:
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References:
[1] W.H. Doherty, "A New High Efficiency Power Amplifier for Modulated Waves," *Proc. Institute of Radio Engineers*, vol. 24, no. 9, pp. 1163-1182, Sept., 1936.
[2] Z. Yu, M. Iwamoto, L.E. Larson, and P.M. Asbeck, "Doherty Amplifier with DSP Control to Improve Performance in CDMA Operation," *International Microwave Symposium Dig. Tech. Papers*, vol. 2, pp. 687-690, June, 2003.

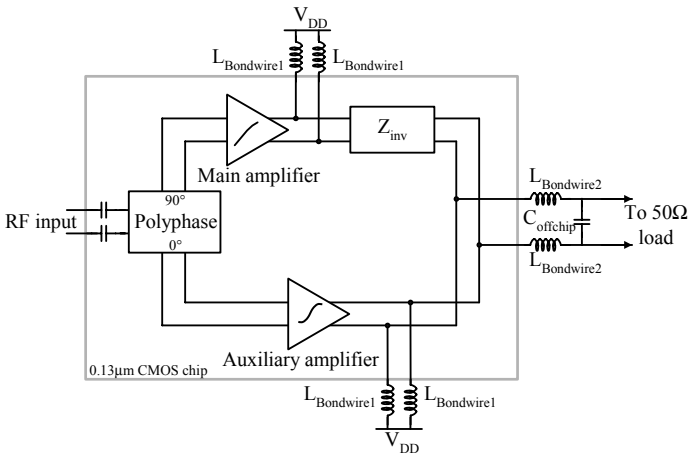

Figure 26.9.1: Block diagram of the CMOS RF Doherty PA.

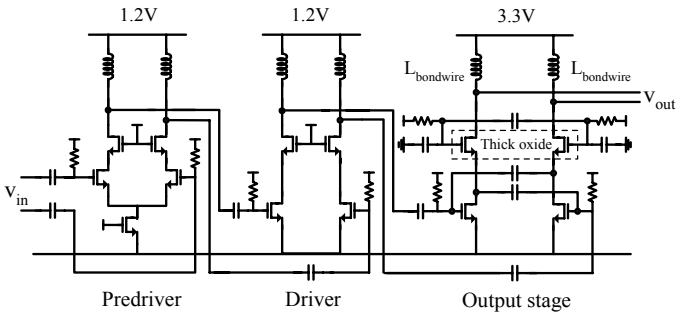

Figure 26.9.2: Main/auxiliary amplifier circuit diagram.

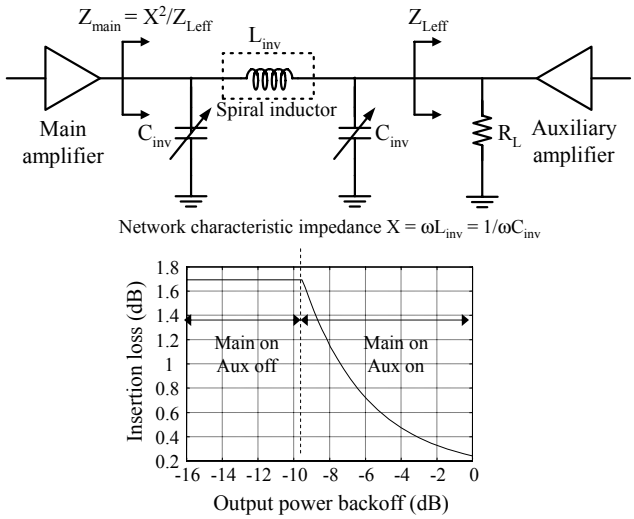

Figure 26.9.3: Passive lumped-element impedance inverter network.

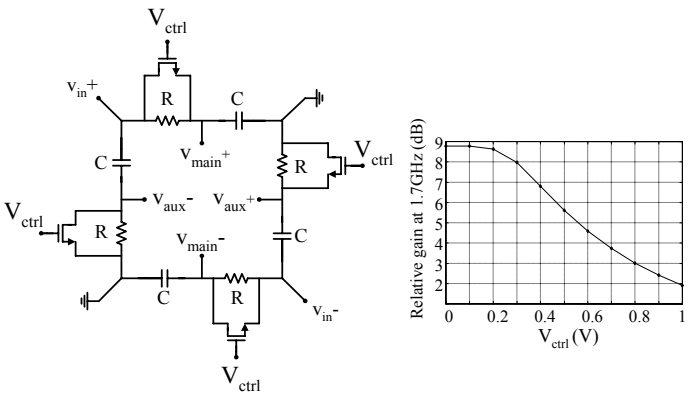

Figure 26.9.4: Polyphasecircuit diagram and gain control characteristic.

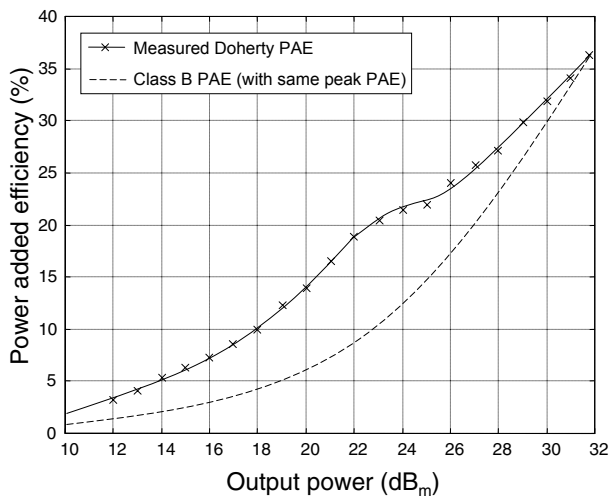

Figure 26.9.5: Measured PAE for different output power levels.

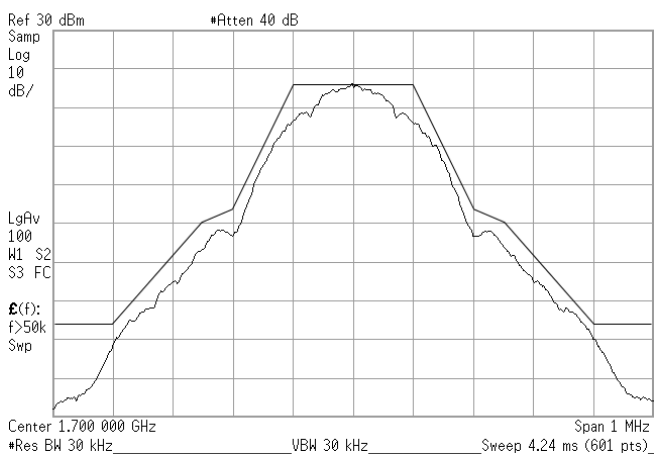

Figure 26.9.6: Measured GMSK output spectrum.

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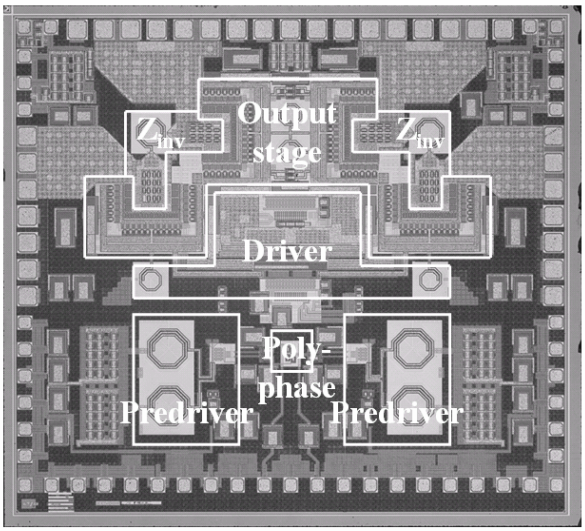

Figure 26.9.7: Chip micrograph of the CMOS RF Doherty.

